Course Code:20CS0504 **R20**

SIDDHARTH INSTITUTE OF ENGINERING & TECHNOLOGY
(Autonomous)
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code: Computer Organization &Architecture(20CS0504) **Year & Sem :** II B.Tech & I-Sem
Course & Branch : B.Tech -CSE,CSM,CIC,CAD,CCC,CSIT **Regulation :** R20

UNIT –I

BASIC STRUCTURE OF COMPUTERS

1	a	Sketch the basic functional units of computer	[L3][CO1]	**[04M]**
	b	Explain the functional units in the computer	[L2][CO2]	**[08M]**
2	a	Differentiate between I/O unit and memory unit.	[L2][CO6]	**[04M]**
	b	Differentiate between Primary Memory and Secondary Memory.	[L2][CO1]	**[04M]**
	c	Differentiate between control unit and ALU	[L2][CO1]	**[04M]**
3	a	Describe the Basic Operational Concepts of computer with neat diagram	[L2][CO1]	**[08M]**
	b	What is the Purpose of PC, IR and General-Purpose Registers.	[L1][CO1]	**[04M]**
4	a	Describe how the Keyboard and Display devices transfer the data with the Processor.	[L1][CO1]	**[06M]**
	b	Discuss about the Program Control I/O and Interrupt I/O	[L2][CO1]	**[06M]**
5	a	List the types of Buses and Give the function of each Bus.	[L2][CO1]	**[08M]**
	b	Give the Structure of BUS Interface with various devices in computer.	[L4][CO1]	**[04M]**
6	a	Identify and explain various Phases of instruction cycle	[L3][CO1]	**[10M]**
	b	List the Classification of Computer Instructions.	[L2][CO2]	**[02M]**
7	a	Discuss any two instructions in each group of Data Transfer, Data Manipulation and Program Control Instructions with example.	[L2][CO1]	**[6M]**
	b	Discuss the Following Instructions with example LD, XCH, OUT, POP, DEC, ADDC	[L2][CO1]	**[6M]**
8	a	Discuss the Following Instructions with example CLR, XOR, SETC, ROL, JMP, CALL	[L2][CO1]	**[06M]**
	b	If Accumulator A =0000 1011, B= 0000 1100 and Carry bit C= 1 then find the value after the execution of the following Instructions i) NEG A ii) ADD A,B iii) SHR A iv) SHLA A v) AND A,B vi) RORC A.	[L2][CO1]	**[06M]**
9	a	What is Addressing Mode and List Different Addressing Modes	[L3][CO1]	**[06M]**
	b	Explain the following addressing Modes with Examples i) Immediate ii) Direct iii) Implied iv) Register Indirect v) Auto increment vi) Relative	[L2][CO1]	**[06M]**

10	Assume that R1 = 400 , 270 in 400 Address, 600 in 500 Address Location. 890 in 600 Location. What is the Data in the Accumulator after the execution of the Instructions. (i) MOV A, R1 (Register Addressing Mode) (ii) MOV A, @ R1 (Register Indirect Addressing Mode) (iii) MOV A, 500 (Direct Addressing Mode) (iv) MOV A, @500 (In Direct Addressing Mode)	[L4] [CO3]	**[12M]**

UNIT –II

DATA REPRESENTATION&COMPUTERARITHMETIC

1	a	List different types to represent Signed Numbers.	[L3][CO3]	**[06M]**
	b	Represent -274 in signed magnitude, 1s complement and 2s complement	[L2][CO3]	**[06M]**
2	a	Subtract 1101 and -1001 using 2's complement subtractions	[L2][CO3]	**[06M]**
	b	Discuss the overflow condition in addition and subtraction	[L2][CO3]	**[06M]**
3	a	What is the General Form of Floating-point representation and give the significance of each part	[L5][CO1]	**[06M]**
	b	Discuss the ASCII Code for the representation of Characters.	[L2] [CO1]	**[06M]**
4		Explain the Flow chart for Addition and Subtraction.	[L2] [CO1]	**[12M]**
5		Discuss the Multiplication algorithm with Shift and add method with suitable flowchart. Multiply the binary numbers (01011) and (01101) Using Shift and add method	[L3] [CO3]	**[12M]**
6		Illustrate the steps in Booth multiplication flow chart. Show the step by step signed multiplication of (-7) and (-11) using Booth algorithm	[L6] [CO3]	**[12M]**
7		Develop and discuss the Flow chart for Division of numbers Give the step by step procedure to Divide 01101010100 with 10001and find the results	[L3] [CO3]	**[12M]**
8		Develop flowchart for the addition/subtraction of floating-point number and illustrate with an example.	[L4][CO3]	**[12M]**
9		Develop flowchart for the Multiplication of floating-point number and illustrate with an example.	[L6] [CO3]	**[12M]**
10		Write an algorithm for the division of floating-point number and illustrate with an example.	[L4][CO3]	**12M**

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UNIT –III

REGISTER TRANSFER & MICROOPERATIONS AND CPU CONTROL UNIT DESIGN

1	a	What is register transfer language and micro operations?	[L2][CO3]	**[02M]**
	b	Design the block diagram of the hardware that implements the following register transfer statement **P: R2←R1.**	[L3][CO3]	**[04M]**
	c	Explain the symbols used in Register Transfer Language.	[L2][CO3]	**[02M]**
	d	What are the different states in 3 state buffers what is the advantage of 3 state buffers.	[L2][CO3]	**[04M]**
2	a	Construct a 4-line common bus system with a neat diagram.	[L3][CO3]	**[06M]**
	b	Explain Bus line with three state buffers.	[L2][CO3]	**[06M]**
3	a	Discuss the any four Arithmetic Micro Operations.	[L3][CO3]	**[06M]**
	b	Draw and explain four bit parallel adder circuit.	[L2][CO3]	**[06M]**
4	a	Draw and explain four bit parallel adder – subtractor circuit.	[L3][CO3]	**[06M]**
	b	Discuss about binary increment with neat sketch.	[L2][CO3]	**[06M]**
5		Explain 4-bit arithmetic circuit which perform all the arithmetic operations	[L2][CO3]	**[12M]**
6	a	Consider A= 0101, then solve the following i) A(2) is selectively reset ii) A(3) is selectively set iii) A(2) is selectively complement iv)A is clear	[L2][CO3]	**[04M]**
	b	Consider A=01101010. Insert 1100 in the lower nibble of A using Masking and Insertion.	[L2][CO3]	**[04M]**
	c	Design Hardware implementation of one stage Logic Circuit	[L2][CO3]	**[04M]**
7	a	Explain the logical shift and arithmetic shift instruction with example	[L2][CO3]	**[04M]**
	b	Draw 4 bit combinational circuit shifter.	[L3][CO3]	**[04M]**
	c	Find the output after performing SHR, ,ASHL,CIR for 10110110 (2)	[L3][CO3]	**[04M]**
8	a	What is Hardwired Control? Explain in detail with a neat diagram.	[L2][CO6]	**[08M]**
	b	Differentiate between Hardwired Control and Micro-programmed control	[L2][CO6]	**[04M]**
9	a	Describe the Micro Programmed Control with a neat sketch.	[L2][CO6]	**[08M]**
	b	What is micro programmed control. List the advantages	[L2][CO6]	**[04M]**
10	a	Define Routine and mapping in address sequencing.	[L2][CO6]	**[04M]**
	b	Describe the Address Sequencing for control memory with neat block diagram.	[L3][CO4]	**[08M]**

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UNIT –IV

MEMORY ORGANIZATION

1	a	What is Cache and Auxiliary memory?	[L2][CO2]	**[03M]**
	b	Sketch the Memory Hierarchy and discuss	[L3][CO3]	**[06M]**
	c	Differentiate RAM & ROM memories	[L2][CO2]	**[03M]**
2	a	Explain 128*8 RAM with block diagram and function table.	[L2][CO3]	**[6M]**
	b	Explain 128*8 ROM with block diagram and function table..	[L2][CO3]	**[6M]**
3		Explain how memories connected with CPU with diagram.	[L2][CO3]	**[12M]**
4	a	Distinguish between SRAM & DRAM.	[L3][CO2]	**[04M]**
	b	Discuss briefly about synchronous DRAMs.	[L2][CO3]	**[08M]**
5	a	Classify the ROM memories.	[L3][CO3]	**[02M]**
	b	Explain different ROM memories	[L2][CO4]	**[10M]**
6	a	What is cache memory What is hit and miss in the cache memory.	[L3][CO4]	**[08M]**
	b	List and Explain different mapping in Cache memory	[L2][CO4]	**[04M]**
7	a	What is Virtual Memory? Discuss how address mapping using pages.	[L2][CO4]	**[06M]**
	b	Explain the relation between address and memory space with an example.	[L2][CO4]	**[04M]**
	c	What is the need of a page replacement? Discuss the LRU page replacement Algorithm with an example.	[L2][CO3]	**[02M]**
8	a	Compare various types of Auxiliary memories.	[L2][CO2]	**[06M]**
	b	Define track and sector. Analyze the importance of auxiliary memory?	[L3][CO3]	**[06M]**
9	a	What is DMA give its significance in data transfer	[L2][CO6]	**[4M]**
	b	Give the significance of different control signals in DMA transfer	[L2][CO6]	**[4M]**
	c	Sketch the block diagram of DMA controller	[L2][CO6]	**[4M]**
10		Give detailed notes on DMA transfers in computer system with neat sketch.	[L3][CO6]	**[12M]**

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UNIT –V

PIPELINIG & PARALLEL PROCESSORS

1	a	Explain the concept of 4 stage Pipelining with diagram.	[L2][CO5]	**[6M]**
	b	How many clock cycles are required to complete n-tasks in k-segment pipeline?	[L2][CO6]	**[2M]**
	c	Compute the required clock cycles in 4 stage pipeline when k=4 , n=6	[L2][CO6]	**[4M]**
2	a	What are the sub operations performed in arithmetic pipelining?	[L2][CO6]	**[4M]**
	b	Sketch the flowchart for floating point multiplication in arithmetic pipeline.	[L3][CO5]	**[6M]**
	c	Calculate the delay time in an equivalent non-pipeline floating point adder subtractor, when t_1=60ns,t_2=70ns,t_3=100ns,t_4=80ns,t_r=10ns.	[L3][CO5]	**[2M]**
3	a	Anticipate three types of hazards (conflicts) in instruction pipelining.	[L3][CO5]	**[06M]**
	b	Define hardware interlock, operand forwarding and delayed load	[L2][CO5]	**[06M]**
4	a	Construct 4-segment Instruction Pipeline and explain.	[L3][CO5]	**[6M]**
	b	Explain the three major difficulties caused by the branch instruction in the instruction pipeline.	[L2][CO1]	**[6M]**
5		Categorize and discuss various forms of parallel processing based on Flynn's Taxonomy with a neat sketch	[L3][CO5]	**[12M]**
6	a	Visualize the characteristics of Multiprocessor and define the technique used to alleviate the problem in single module.	[L2][CO5]	**[6M]**
	b	Explain the following with neat sketch i) UMA Multiprocessor ii) NUMA multiprocessor	[L2][CO5]	**[6M]**
7	a	Define interconnection network, bandwidth and effective throughput.	[L2][CO6]	**[6M]**
	b	Explain the bus in interconnection network.	[L2][CO6]	**[6M]**
8	a	How the ring network is formed?	[L2][CO6]	**[2M]**
	b	Explain the two ways to mitigate the high latency in ring network with neat sketch.	[L2][CO6]	**[10M]**
9	a	Explain cross bar switch with neat sketch.	[L2][CO6]	**[6M]**
	b	Explain 2D mesh network with neat diagram.	[L2][CO6]	**[6M]**
10	a	Explain the following in the write through protocol. i) Update ii) Invalidation	[L2][CO6]	**[6M]**
	b	Explain in detail about the snoopy cache.	[L2][CO6]	**[6M]**

Prepared by:
1. Dr. Madhusudan, Professor /ECE
2. Mr. A.VijayaPrabhu, Associate Professor /ECE
3. Mrs G. Priyanka, Asst. Professor /ECE
4. Ms. M. Diana Amutha Priya, Asst. Professor/ECE

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